REMARKS

The Examiner is thanked for her careful and very thorough Office Action. The Examiner is particularly thanked for the helpful suggestions regarding correction of the alleged informalities. The present Proposed Amendment is submitted to provide a simple way to obtain allowance of all rejected claims. (Applicant expressly reserves the right to present the same or broader claim scope again in a continuing application, and notes that no subject matter is being disclaimed by the present amendment.)

Claims 1-7 have been rejected. By the foregoing amendments, various Claims are sought to be amended or canceled without prejudice or disclaimer.

Note that the amendments to Claims 3-5 are intended to be purely formal amendments, and are believed not to change the scope of these claims.

The amendment to Claim 1 is not intended to be substantive. Claim 1 is being amended for clarification purposes. The support for amended Claim 1 and added Claim 8 can be found in the paragraph beginning on line 30 of page 10.

The term "map level identifier" is used to denote the level of detail. This can be found in line 31 of page 10 of the present application.

By the amendment filed on April 9, 2003, the description for the equations in Claim 6 can be found in the paragraphs added after line 15 of page 75.

The foregoing amendments to the specification are submitted to improve clarity, and to remove various typographical and other minor informalities. These changes are respectfully asserted not to introduce new matter, and their entry is respectfully requested.

The Examiner has suggested that the term "tag" used in the claims is inconsistent with the specification. Applicant respectfully requests that the Examiner state how this term is being used inconsistently.

Art Rejections

The art rejections are all respectfully traversed.

Rejections Under 35 USC 102(b)

Claims 1-7 stand rejected under 35 USC Section 102(e) as being anticipated by *Duluk, Jr. et al.*

Claim 2 has been canceled without prejudice by the above amendment. The rejection of this claim is traversed and is now believed to be moot.

Duluk, Jr. et al. relates to a deferred graphics pipeline processor. It does not appear to teach or suggest the generation of condensed cache tags.

The claim language of amended Claim 1 is not met. Specifically, Claim 1 now recites "**generating condensed cache tags, by removing two bits from the tag length by means of a remapping which exploits the different address resolutions implied by level of detail settings in the different mip mapping processes to re-encode the mip mapping addresses.**" As stated in the present application:

> **...Each texel can therefore be uniquely identified by its index and map level or (i, j, map). If the tag or key is made up out of these three items then no address calculations are needed in order to carry out the search.**
>
> **The key can be the concatenation of these three values and this will give a key of (12 + 12 + 4) bits, as the maximum texture map size is 2Kx2K with a border. A key size of 28 is larger than preferred, as the Content Addressable Memory (CAM) used to implement the parallel search is expensive. If the highest resolution map is 2Kx2K then in a mip map chain, the next map will have a resolution of 1Kx1K, then 512x512, etc.**
>
> **Also there are two independent caches (they can be combined, but this is ignored here), and when mip mapping, the even maps are directed to one**

cache and the odd maps to the other cache. This means that in the worst case the even cache needs to simultaneously differentiate between texels on the level of 2K, 512, 128, etc. resolution maps.

The texture is held in 2x2 patches within the cache so the least significant bit of i and j have no use, so these can also be discarded.

These ideas can be used to reduce the size of the key to 23 bits, as a different algorithm is used to generate the key for the different map levels 0, 1, 2 and (3...11).

Thus, in this sample embodiment, the tag length derived from (i, j, map) inputs is reduced (e.g. from 28 to 23) by:

splitting odd/even maps into two banks (already done for other reasons (viz.: 1. for mip mapping with high quality, we are always accessing texels from both an even level and an odd level; and 2. for applying more than one texture map, the two separate maps are referenced separately);

ignoring *least significant bits of i and of j, due to the use of 2x2 patches; and*

getting two more bits from a remapping, which exploits the different address resolutions implied by level of detail settings in the different mip mapping processes to re-encode the mip mapping addresses into a length which is only one bit longer than the max condensed length of x and y addresses.-

Duluk, Jr. et al. does not disclose or suggest condensing cache tags by getting two more bits from a remapping. As acknowledged by the Examiner, *"Duluk has also disclose 4 bit field for LOD and 11 bits field f r tex ure coordinates which is a total of 26 bits for a tag." Duluk, Jr. et al.* red es a 28 bit tag to a

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26 bit tag by using a cache line that holds a 2x2 patch to reduce the indices by one bit to 11 bits. However, the inventions disclosed by the present application not only condense a 28 bit tag to a 26 bit tag by using a cache line that holds a 2x2 patch, but also further condense the tag to a 23 bit tag by performing a remaping. As stated in the present application:

> **The key (as already described) holds the i and j index and the map level (3D textures will be considered shortly). The maximum width and height of a map is 2050 (2K + a border) so the indices have 12 bits. The cache line holds a 2x2 patch so the indices can be reduced by one bit to 11 bits. The number of map level is needed here. In total the key is (11 + 11 +4) bits or 26. This can be reduced down to 23 by realizing that the full 2050x2050 value can occur on map level 0. Map level 1 has a maximum size of 1026x1026 so by encoding the map into the upper bits as shown in Figure 8, the key width can be reduced.**[2]

Duluk, Jr. et al. does not disclose or suggest this further step of remapping.

According to the Federal Circuit:

> **For a prior art reference to anticipate a claim, the reference must disclose each and every element of the claim with sufficient clarity to prove its existence in the prior art.**[3]

Accordingly, Applicant respectfully requests withdrawal of this rejection.

Claim 3 also recites features not shown or suggested by *Duluk, Jr. et al.* Specifically, Claim 3 recites "**caching texture memory fetches using a cache tag assignment in which a unique relation between a mip-mapping-level-of-detail**

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[2] Page 24, line 32 to page 25, line 5.
[3] Motorola, Inc., v. Interdigital Tech. Corp., 43 USPQ 2d 1481, 1490 (Fed. Cir. 1997).

parameter and coordinate bits defines a smaller tag address for any given memory address." As stated earlier, *Duluk, Jr. et al.* only teaches using a cache line that holds a 2x2 patch to reduce the indices by one bit to 11 bits. *Duluk, Jr. et al.* does not disclose or suggest using a unique relation between a mip-mapping-level-of-detail parameter and coordinate bits to define a smaller tag address for any given memory. Therefore, for this reason and the reasons discussed above, Applicant respectfully requests withdrawal of this rejection.

Claim 6 also recites features not shown or suggested by *Duluk, Jr. et al.* Specifically, Claim 6 recites "**coding said map level identifier so that the largest map level uses 1 bit to designate the map level and ((m-i) + (n-j)) bits to specify said addresses on said x- and y-axis, the second largest map level uses 3 bits to designate the map level and ((m-i) + (n-j)-2) bits to specify said addresses on said x-axis and y-axis, and successively smaller map levels use greater than 3 bits to designate the map level and less than ((m-i) + (n-j)-2) bits to specify said addresses on said x-axis and y-axis.**" *Duluk, Jr. et al.* does not disclose or suggest this step of coding. Therefore, for the reasons discussed above, Applicant respectfully requests withdrawal of this rejection.

Claim 7 also recites features not shown or suggested by *Duluk, Jr. et al.* Specifically, Claim 7 recites "**a direct-mapped texture cache for said texture memory, configured to be accessed using lookup tags which require m + n - 1 or fewer bits.**" Because m and n represent arbitrary index values, each value is 12 bits making the lookup tags 23 bits or fewer. As stated earlier, *Duluk, Jr. et al.* does not disclose or suggest condensing cache tags to 23 bits. Therefore, for the reasons discussed above, Applicant respectfully requests withdrawal of this rejection.

Finally, dependent Claims 2, 4, and 5, which depend directly from independent Claims 1 and 3 and incorporate all the limitations thereof, also

include additional limitations that are not shown or suggested by *Duluk, Jr. et al.*

Claim 4 recites "**said cache tag assignment is generated by combining a mip-map-level-of-detail parameter which can have at least 2^{J-1} + 1 different values together with coordinate bits which can have as many as 2^{K} different values into fewer than J + 2K bits without loss of information; wherein J represents the number of bits for the level of detail and K represents the number of bits for arbitrary coordinate values.**" Because K represents the number of bits for arbitrary coordinate values (11 bits), and J represents the number of bits for the level of detail (4 bits), the present inventions disclose a condensed cache tag of less than 26 bits. As acknowledged by the Examiner, *Duluk, Jr. et al.* discloses 26 bits for a tag. It does not suggest or disclosed a tag that is less than 26 bits.

Claim 5 recites "**said cache tag assignment is generated by combining a first parameter which can have at least 2^{J-1} + 1 different values together with coordinate bits which can have as many as 2^{K} different values into fewer than J + 2K bits without loss of information; wherein said first parameter and said coordinate bits are three-dimensional coordinates; and wherein J represents the number of bits for the level of detail and K represents the number of bits for arbitrary coordinate values.**" As stated above, the present inventions disclose a condensed cache tag of less than 26 bits. *Duluk, Jr. et al.* not suggest or disclosed a tag that is less than 26 bits.

Thus, for this reason, and for the reasons discussed above, Applicant respectfully requests withdrawal of this rejection.

Conclusion

Thus, all grounds of rejection and/or objection are traversed or accommodated, and favorable reconsideration and allowance are respectfully requested. The Examiner is requested to telephone the undersigned attorney for an interview to resolve any remaining issues.

Respectfully submitted,

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